After Sales Technical Documentation

THX–4 Series Transceiver

Chapter 4

SYSTEM MODULE

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CHAPTER 4 – SYSTEM MODULE

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Introduction

General

The system module controls the operation of the internal parts of the phone. Its task is to control the user interface, i.e. LCD driver, keyboard, and audio interface functions. The module performs all signalling towards the system and carries out audio–frequency signal processing. In addition, it controls the operation of the transceiver and stores tuning data for the phone.

The RF unit receives and demodulates the radio frequency signal from the base station and transmits the modulated signal to the base station.

Special Features

- Accessory connector at bottom, e.g. for RF booster and handsfree units.
- RF connector at bottom, with RF switch for connection to accessories.
- Extra lines to processor and ordinary lines with additional functions to communicate with accessories.

Technical Specifications

Modes of Operation

The module has two active operating modes as follows:

- Conversation mode
- Listening mode

In the conversation mode all IC's are active.

In the listening mode some blocks of the audio IC NANTIC are in standby state. The transmitter and its synthesizer are switched off.

External Signals and Connections

The module has two external connectors, the system connector and the display module connector. The system connector incorporates the charging connector, the accessory connector and the external antenna connector.

System Connector J1

Pin	Name	Description
1	VC	Charger Input +ve
2	XEXAUD	Booster power control output.
3	HOOK	On hook indication for auxillary handset.
4	XEAR	External earphone signal.
5	0V	0V for both charger and audio.
6	VC	Charger input +ve
7	MBUS	Bidirectional asynchronous data bus.
8	0V	0V for both charger and audio
9	XMIC	External microphone signal
10	0V	0V for both charger and audio
11	0V	For charger
12	VC	Charger input +ve
13	VC	Charger input +ve
14	0V	0V for charger
15	0V	0V
16	RF	RF signal to duplex filter
17	RF	RF signal to antenna
18	0V	0V
19	VBAT	Battery voltage
20	BTEMP	Battery temperature measurement, 27k pull–up resistor to 4.8V.
21	BSI	Battery size indication, 100k pull–up resistor to +4.8V
22	0V	0V for battery

Display Module Connector J2

Pin	Name	Description
1	ROW1	Row 1 of keypad matrix
2	COL0	Column 0 of keypad matrix
3	ROW0	Row 0 of keypad matrix
4	COL3	Column 3 of keypad matrix
5	VBAT	Battery voltage power for LED’s
6	LCD LIGHTS	Current supply for LCD backlights
7	LCD_CLK	Clock for LCD driver
8	LCD_RES	Reset for LCD driver
9	XLCDEN	LCD driver for chip enable
10	C_XD	Command/No data
11	SCL	Serial data clock
12	VL2	Supply voltage for LCD driver
13	XBUSY	Busy signal from LCD driver
14	0V	0V power connection
15	SDA	Serial data
16	V_LCD	Negative voltage for LCD
17	EARP	Earpiece connection (not used)
18	EARM	Earpiece connection (not used)

Internal Signals

Connections between RF and Baseband

Name	Function
DAF	RX audio and data
IF_FREQ	2nd IF input
VTCXO	VTCXO control signal
RSSI	Received signal strength indicator
V_REF	Voltage regulator reference, 4.85V nominal
MOD	Transmitter modulation signal
V_ALC	Power control input
TXI	Transmitter power indicator
VBAT	Battery voltage
–VMOD	Negative bias voltage for modulation diode
5VRXEN	RX regulator on/off
PAV_EN	Power amplifier on/off
SYNDAT	Serial data for synthesiser
SYNCLK	Serial clock for synthesiser
RXLE	Rx synth latch enable
TXLE	Tx synth latch enable
VDRIVER_EN	Tx power rail enable

Functional Description

Logic Circuit Description

General

The audio/logic unit consists of 5 IC's: controller D404, modem N403, audio NANTIC N408, EEPROM D406, regulator PSL N407.

Micro–controller

Micro–controller D404 has six 8–bit I/O ports (Ports 1, 3, 4, 5, 7 and 9), one 5–bit port (Port 2), one 4–bit I/O port (Port 6) an 10–bit 8–channel A/D converter (Port 8), three PWM timers, serial communication interface. All memory (62 kB ROM, 2 kB RAM), except EEPROM, is located in the micro–controller.

Micro–controller D404 Pinout

Pin	Name	Description
1	R_XW	Address Bit for Modem
2	XCS	Chip Select for Modem
3	XRD	Read Control to Modem
4	XWR	Write Control to Modem
5	VCC	Logic Supply Voltage VL1
6–8	MD0–MD2	Mode Selection
9	XSTBY	HW Standby Mode input from PSL
10	XRES	Reset from PSL
11	NMI	Modem Interrupt
12	VSS1	Ground
13–20	D0–D7	Data bus for modem
21	PDB2	bit 2 of the predriver bias adjustment
22	PDB1	bit 1 of the predriver bias adjustment
23	PDB0	bit 0 of the predriver bias adjustment
24	PAB2	bit 2 of the power amplifier bias adjustment
25	PAB1	bit 1 of the power amplifier bias adjustment
26	PAB0	bit 0 of the power amplifier bias adjustment
27	XBIAS	PA and predriver bias voltage switch
28	VDRIVER_EN	RF power supply control switch
29	VSS2	Ground

Pin	Name	Description
30–36	ROW 0–6	Keypad inputs
37	OUT_T	Buzzer Volume Control
38	COL 0	Keypad outputs and power up control
39–41	COL 1–3	Keypad outputs
42	VCC2	Logic Supply Voltage VL1 Input
43	SYNDAT	Serial data for RF synthesizers
44	LIGHTS	Output to turn ’on’ the LED’s
45	RXLE	Latch enable for RX synthesizer
46	MBUSNF	MBUS input
47	TXLE	Latch enable for the TX synthesizer
48	5VRXEN	RX RF supply switch control
49	SIS RST	SIS chip reset
50	PAV_EN	PA supply switch control
51	Avss	Ground
52	VBATSW	Battery voltage monitor
53	CHRGMON	Battery charge monitor
54	RSSI	Received signal strength indication
55	TXI	Transmitter indication
56	BTEMP	Battery temperature
57	AD_5	Hook detection input from accessory
58	BSI	Battery size indication
59	HFJCON	Handsfree junction box sense
60	AVCC	A/D Convertor reference voltage VREF
61	ANTSDA	N_ANTIC Serial Data
62	SDSI	Interim ESN Security Line
63	XEXAUD	PWM output to accessory connector
64	VTCXO	Frequency trim control voltage for TCXO
65	CSW	Pulse width modulated charger control
66	TXD	Transmit serial data to M2BUS
67	RXD	Received serial data from M2BUS
68	SCL	Synchronous clock from EEPROM and LCD data
69	EXTAL	External signal clock from modem
70	XTAL	Not Used
71	VSS3	Ground

Pin	Name	Description
72	ACLK	Clock for NANTIC
73	XBUSY	Busy signal for LCD driver
74	XLCDEN	LCD driver IC select
75	C_XD	LCD driver and EEPROM multiplex control
76	CSCK	NANTIC and SIS serial interface clock
77	SYNCLK	Synthesiser serial data clock
78	NMI	Modem interrupt
79	SDA	Serial data to EEPROM and LCD–driver
80	XAS	Address bit for Modem

Modem

The NAT (N403) is a single VLSI chip modem for the AMPS/TACS mobile telephone. It implements a Manchester data receiver–transmitter, and provides supervisory audio tone (SAT) and signalling tone (ST) functions. Received messages are corrected and checked by 3/5 voting and BTH decoding blocks.

Modem (N403) Signals

Name	Description
INT	interrupt output to controller
XCLR	reset input
XCS	chip select from controller
D0–7	data bus to controller
A0–1	address lines for register selection
XRD, XWR	read/write control from controller
DI	data input from RF unit
DO	data output to ANTIC
C1–2	clock generator
CLOCKOUT	system clock output to controller and SIS
DAC 0	dac o/p to VALC

Regulators

Regulator PSL (N407) is the power supply circuit for battery operated applications requiring separate voltage supplies (for the microcontroller, logic and analogue functions). It has three voltage regulators (VL1, VL2 and VA), a reference voltage output (VREF), power on/off and reset logic, and a watchdog, in addition to circuitry for supply voltage and battery charger monitoring functions.

PSL N407 Signals

Name	Description
VBAT	battery voltage input
VREF	voltage reference output (+4.85V ±2 %)
VL1	logic voltage output (+4.85 V) for controller
VL2	logic voltage output (+4.85 V) for other logic
VA	analogue voltage output (+4.85 V)
VBATSW	switched VBAT voltage
XPWRON	power on control input from key-board
XPWROFF	power off control from controller (watchdog)
XRESET	reset control output for logic
XSTBY	standby control for controller
CHRGDET	battery charger detection input
DETIN	supply voltage detection input
CRESET	connection for external timing ca-pacitor defining reset signal delay
COFF	connection for an external timing capacitor defining power off delay
CPOR	connection for external capacitor for controlled power on master re-set
GND	ground (analogue/logic)

Memories

EEPROM D406 comprises nonvolatile memory into which is stored the tuning data for the phone. In addition, D406 contains 99 short code memory locations to retain user selectable phone numbers. EEPROM data signal SDA is fed to the display modules multiplexer, where the signal is divided into two SDA lines.

EEPROM D406 Signals

Name	Description
SCL	IIC bus clock
SDA_2	IIC bus data

Charging Control

The circuit is basically a power switch, V403, which connects an external constant current source to the battery. V403 is driven by a modified long tail pair (emitter–coupled pair) which provides a safety mechanism to stop excessive voltages being placed across the phone's internal circuitry. This long tail pair consists of V420 and V421 in a negative feedback configuration, with the control input applied to the base of V421 and the feedback to the base of V420. The potential divider R465 // R514 and R464 is used to scale the voltage on the anode of diode V508 and place it on the base of V420. By long tail pair action, the divided voltage will be the same as the base voltage of V421, and the voltage applied across the battery is therefore clamped. Note, however, that this clamping only takes place under fault conditions.

When V403 is switched on, the parallel combination of R467 and R468 provide sufficient base current to ensure that it is in a state of saturation. The switching circuit is normally controlled by the microprocessor's CSW output (P94–SCK2_PW13) which drives V421 via smoothing circuit R466, C461 and R470. However, at power up (i.e. the insertion of the battery or of a charger), the PSL overrides it for a period of about 1s by holding the XRES line low.

The voltage at which the battery is clamped can be set to one of three levels by using the PAV_EN line to switch V406B and the XRES line to switch V406A. When charging normally, the processor's CSW line is at 4.8V nominal and the resultant maximum voltage on the battery will be 11.2V. During a call, however, PAV_EN is asserted and the effect of R456 on the division ratio is consequently removed, causing the limiting voltage on the battery to become 8.8V. During reset, the Zener diode V506 places 2.6V on the base of V421 and the battery voltage will then not be able to exceed 6.5V.

Once fully charged, the CSW line is switched using PWM for battery maintenance.

Display Lighting

Control of the keyboard display lighting is performed by V700, R716 and R713; control of the LCD lighting is performed by V701, R705 and R716. All lighting is enabled by a high level on pin 44 (P71) of D404.

Audio Circuit Description

Transmit (TX) Signal Path

The TX audio signal is processed in the NANTIC and fed, via the MOD line, to the synthesizer. NANTIC contains the following stages for TX signal processing:

Name	Description
MICAMP	Signal from the microphone is fed to this stage and amplified
MUX	TX source selection (EXMIC/MIC/DTMF/MUTED)
TXAAFIL	Anti alias filter (see NANTIC specification)
BANDPASS	(see NANTIC specification)
TXATT	For handsfree mode of operation
COMPRESSOR	2:1 syllabic compressor
PREEMP	Pre–emphasis filter
AGC	Soft Limiter
LIMU	Hard limiter
LOWPASS	Low pass notch filter
POSTFIL	Second order Sallen–Key filter
SUMSTAGE	Data from modem is summed in here
TRCOMP	Modulation sensitivity compensation

Receiver (RX) Signal Path

The demodulated audio signal (DAF) from the receiver is fed to the NANTIC circuit which contains a software controlled receiver and compensation amplifier. The output of this stage drives the modem IC and the remaining NANTIC RX signal processing stages.

Name	Description
MUX	RX source selection (DTMF/DAF1/DAF2)
RXAAFIL	Anti alias filter
RXFIL	Second order Sallen–Key filter
EXP	2:1 Syllabic Expander
VOLUME	Volume Control Amplifier
RXATT	For Handsfree mode
EARPAMP	The earphone amplifier is a single input, differential output amplifier for a ceramic earpiece
ACCAMP	Accessory amplifier – buffer for XEAR output

RF Circuit Description

Receiver Signal Path

The receiver is a dual–conversion superheterodyne with the intermediate frequencies 45 MHz and 450 kHz.

The RF signal from the Antenna is first filtered from the Transmitter Signal by the Duplex Filter. It is then applied to V1 the Low Noise Amplifier (LNA). This amplifies the signal to a level sufficiently high to overcome the conversion noise of the First Mixer N8. In order to reduce the level of the Transmitter Signal and spurious responses reaching the First Mixer, an Interstage Surface Acoustic Wave (SAW) Filter (Z5) is used between the LNA and First MIxer.

The First Mixer comprises a doubly balanced Gilbert Cell. The balance to unbalanced transformation on the RF Input Port is made with a printed microstrip Balun Transformer. The intermediate frequency (IF) output is transformed using a conventional transformer (L9). In order to tune out the component tolerances of N8, L9 and the IF Filter (FL2), a Varicap Diode V202 is used. The tuning voltage for V202 is derived from a three bit resistive ladder DAC (R1, R33, R38, R39, R74, R75) formed by the Output Ports of the Synthesizer Chips N2 and N12. The Mixer current is boosted in ”Transmit Mode” by V2 in order to maintain performance in the presence of a large (transmit) signal. The Base of V2 is driven internal to the RF sub system by V_DRIVER.

The First IF Frequency is generated by injecting the First Local Oscillator at Frx + 45MHz to the Local Oscillator Port of N8.

The First IF of 45MHz is filtered by the Crystal Filter FL2 which provides attenuation of the Second IF Image Response and filters high level adjacent channel signal from the Second Mixer.

The remaining RX / RF processing is performed by an integrated receiver IF chip N1. The Chip contains a second mixer, an IF amplifier, a limiting amplifier, a quadrature detector and an AF buffer amplifier. The chip has a voltage gain in excess of 100dB turning the microvolt input level into 0.3V signal at the Limiter Output.

The Second Local Oscillator is produced by tripling the Voltage Controlled Temperature Compensated Crystal Oscillator (VCTCXO) at 14.85MHz in V9. The output of the Tripler is tuned to the third harmonic of the input by L7 and C62 at 44.55MHz. The frequency of the VCTCXO is controlled by a PWM DAC within the Baseband Circuitry. The calibrated frequency is set by a value in EEPROM.

The channel bandwidth of the Receiver is determined by the 450kHz Ceramic Filter Z3. This filter provides the majority of the rejection at adjacent and alternate channels.

The Quadrature Phase Shift Network for the Detector L2, C75 and C73 is designed for low Q and close tolerance to eliminate the need for adjustment during manufacture or service.

Received Signal Strength Indicator (RSSI) is derived internally in N1 and is fed directly to one channel of the ADC input on D404.

Synthesizers

Both the Transmitter (N2 and N4) and Receiver (N7 and N12) Synthesizers are dual modulus types with VCO's operating at final frequency. In the case of the Receiver the LO operates at Frx + 45MHz and in the Transmitter the VCO operates directly at the TX frequency. The Prescaler Chips N4 and N7 divide the VCO input by 128/129 to drive the PLL chip. In the PLL chip the reference frequency from the VCTCXO is divided down to the Phase Detectors comparison frequency (12.5kHz) and compared with the divided down VCO frequency.

NOTE: The phase Detector operates at different frequencies for each system protocol (for TACS, the figures are 12.5 kHz Tx and 12.5 kHz Rx).

The loop dynamics are determined by the Loop Filter (TX: C4, C8, R4,) (RX: C54, C55, C103, R31). The Loop Bandwidth is designed to optimise switching time, modulation bandwidth and phase detector sideband attenuation.

The PLL counter values (to determine the synthesiser frequencies) are programmed via a 3–wire serial bus; a status word can also be sent to control the Output Ports, Phase Detector Gain, and Negative Voltage Generator. The port outputs are used to control other RF sub system functions. The status of the synthesiser lock is also read using this bus.

The RX Synthesiser (N12) also provides the negative bias for the PA from its internal invertor pin 13. Multi–function port 1 (MF01) provides the LSB of the 3 bit IF tune DAC.

The Transmitter Synthesiser additionally provides two output ports – MF01 and MF02 which provide bits 2 and 3 of the 3 bit DAC respectively.

VCO's and Buffers

Both VCO's are Colpitts types using a printed microstrip resonator. The Tx VCO is buffered by V3 and V4; the Rx VCO is buffered by V5.

Transmitter

The Transmitter comprises TX buffers PA and ALC. The 0dBm level from the VCO is buffered by V3 and V4 which provides > 60dB of reverse electrical isolation. The isolation is required to ensure impedance changes in the PA Strip are isolated from the VCO (especially important during critical power up timing). The Buffers have a unity gain.

The final two stages of the PA use Gallium Arsenide (GaAs) technology to maximise efficiency. Because of the 'spread ' inherent in GaAs devices, provision has been made to trim the DC bias point of both the driver and PA stages using discrete DACs based around V413 and V415 driven from the port of D404. Microstrip components are used to form low loss matching networks.

The PA output from V7 is fed through a directional coupler embedded within the PCB. This detects a fraction of the transmitter power (–16dB) for the Automatic Level Control (ALC) circuit. A negative voltage proportional to TX power is compared to V_ALC in N10 to produce a DC feedback voltage VALC which is applied to V11. The different power levels are set by using calibration values in EEPROM which are factory set during production alignment.

Duplexer and Spurious Rejection

The Transmitter output level at full power is ≈ +28dBm to the antenna. The Receiver sensitivity is < –110dBm for 20dB SINAD. In order to operate together in duplex mode, more than 140dB ($1x10^{14}$) of filtering and screening is required. The Duplex filtering (Z4) is achieved with helical filter technology in a pre–aligned filter. As well as separating the TX and RX components, the Duplexer also removes transmitter noise from the Cellular Receive Band. Filtering of unwanted harmonics from the Transmitter, and radiation of the RX Local Oscillator from the Receiver is also accomplished.

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